Linearity Analysis of Multi-loop Regulation Voltage Reference Based on GaN MIS-HEMTs

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Abstract

Wide-bandgap gallium nitride devices offer a high critical field, good thermal conductivity, and fast switching, enabling high-voltage, high-temperature applications. This work introduces a generic multi-loop regulated voltage reference topology on a monolithic AlGaN/GaN MIS-HEMT consisting of a D-mode and multiple E-modes. A 4-Transistor implementation produces a stable 2.33 V V_{ref} across a 2.8~50 V V_{DD} supply while achieving an extremely low line sensitivity of 1.27×10^{-10} %/V. Closed-form analytical expressions for reference voltage, line regulation, and start-up voltage are derived to reveal parameter dependencies. These analytical results provide systematic guidance and practical design insights for GaN-based voltage references in high-voltage sensor biasing, power-integration modules, and next-generation intelligent power converters.

Keywords—*GaN, MIS-HEMT, voltage reference, line sensitivity, multi-loop regulation, closed-form derivation.*

I. Introduction

Gallium nitride (GaN) devices, owing to their high critical electric field, superior thermal conductivity, and outstanding high-frequency switching performance, hold significant application potential in smart power conversion, high-voltage, and high-temperature environments [1]-[3]. Currently, the ever-increasing demands of electric vehicle power electronics for supply voltage stability and wide temperature tolerance impose more stringent design challenges on reference voltage generation circuits [4]. The AlGaN/GaN-based metal–insulator–semiconductor high-electron-mobility transistor (MIS-HEMT) employs a gate dielectric to suppress leakage and stabilize threshold voltage, boosting noise immunity and thermal robustness [5].

However, existing GaN-based voltage references (VR) suffer from insufficient linearity, resulting in pronounced output drift under supply-voltage fluctuations. In contrast, CMOS-based solutions, despite their advantages in integration, power consumption, and cost, are constrained by narrower operating voltage and temperature ranges, making it difficult to accommodate both wide input swings and high-temperature stability [6]-[8].

In this work, Keysight's Advanced Design System (ADS) was used to perform circuit-level simulations employing the AlGaN/GaN MIS-HEMT ASM model to realize a high-linearity, multi-loop regulation voltage-reference topology. The proposed topology comprises an enhancement-mode (E-mode) MIS-HEMT and multiple depletion-mode (D-mode)

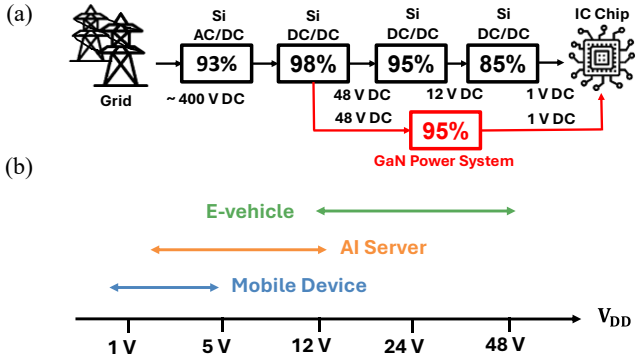


Fig. 1. (a) Schematic diagram of efficiency improvement of GaN technology in power conversion systems. (b) Typical source voltage of power conversion systems.

MIS-HEMTs arranged in a multi-stage reference-voltage chain, thereby exploiting the high transconductance g_m and low output conductance g_{ds} inherent to GaN devices.

II. Working Principles of Multi-Loop Regulation

The topology of the implemented circuit is illustrated in Fig. 3. At its core lies a traditional two-transistor (2T) structure (highlighted in gray), where M_1 is an E-mode device and M_2 is a D-mode device [4][5]. During operation, M_1 functions as a current source, while M_2 is diode-connected with its source grounded. The output voltage V_{ref1} is extracted from the node between M_1 and M_2. This structure exhibits line sensitivity (LS) of V_{ref1} to variations in V_{DD}, since the drain current I_{DD} of M_1, operating in saturation, is influenced by the Early effect and thus depends on V_{DS2}, where $V_{DS2} = V_{DD} - V_{ref1}$ [9].

To mitigate this sensitivity, a regulating transistor M_3 is cascaded at the drain of M_2. The gate of M_3 is connected to the preceding output V_{ref1}, and the new output voltage V_{ref2} is taken from the node between M_2 and M_3. When V_{DD} increases, I_{DD} also increases, causing V_{ref1} to rise. M_3, acting as a source follower, has its source voltage connected to the drain of M_2, which rises in tandem with V_{ref1}. This reduces V_{DS3} and subsequently decreases I_{DD}, thereby pulling V_{ref1} back toward its original value. The opposite response occurs when V_{DD} decreases, sharing the same drain current and operating at identical bias points. The N−1 loop added E-mode transistors (M_3 to M_{N+1}), all share the same aspect ratio as M_2. To clarify, N denotes the number of transistors excluding M_1, representing the total number of E-mode devices. As a result, the source-to-gate voltages of transistors M_3 and M_2 are equal, and both are equal to the reference voltage V_{ref1}. Furthermore, the drain-to-

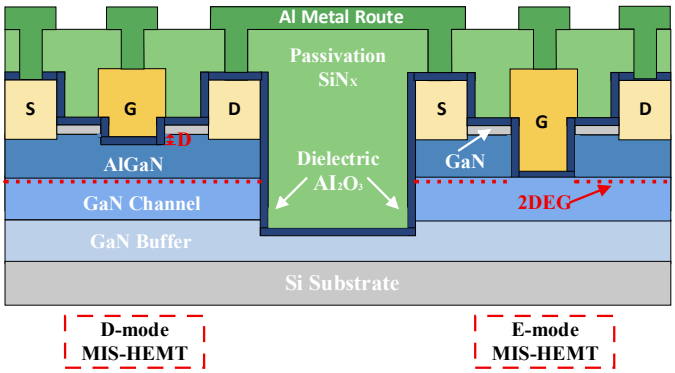


Fig. 2. Cross-section view of GaN D/E-mode MIS-HEMTs.

source voltage of transistor M_2 is equal to the source-to-gate voltage of M_3, so it follows that V_{DS2} is now regulated by V_{ref1}. From the circuit relationship, $V_{DS2} = V_{ref2} - V_{ref1}$, hence $V_{ref2} = 2V_{ref1}$. Extending this analysis to higher-order regulation loops, the final output V_{refN} can be expressed as $V_{refN} = NV_{ref1}$ [10]. Therefore, within the overall circuit logic, the core 2T output V_{ref1} undergoes N−1 rounds of voltage regulation, V_{ref2} undergoes N−2 rounds, and so on, until the final output V_{refN} is not involved in any regulation loop and thus exhibits the highest line regulation (*LR*). Consequently, V_{ref1} achieves the lowest *LR* among all outputs.

III. Simulation Results & Analytical Derivations

All simulations in this work were performed in the Keysight ADS environment using the AlGaN/GaN MIS-HEMT ASM model at temperature of 25 °C. The key device parameters are as follows: D-mode threshold voltage $V_{th,D}$=-2.3 V, E-mode threshold voltage $V_{th,E}$=2.3 V; D-mode gate width W_D=50 μm, E-mode gate width W_E=100 μm.

Fig. 4(a) presents the loop activation and output stability of the 4T architecture versus V_{DD}: When V_{DD} < 5 V, no loop is active and only V_{ref1} is produced (blue region); For 5 V ≤ V_{DD} < 7.3 V, the first loop activates and V_{ref2} is produced (orange region); For V_{DD}≥ 7.3 V, the second loop activates and V_{ref3} is produced (green region). Linear regulation result of V_{ref1} = 2.33 *V* while each loop activates: $LR_{V_{ref1,1}}$=1.79×10^{-3} %/V, $LR_{V_{ref1,2}}$ =4.72×10^{-7} %/V and $LR_{V_{ref1,3}}$ =1.27×10^{-10} %/V. These results indicate the 4T multi-loop architecture achieves the lowest *LR* for V_{ref1}, which means the most stability under the present simulation conditions.

Based on the operating curve in Fig. 4(a), Fig. 4(b) provides a cross-comparison of *LR* and minimum usable V_{DD} to illustrate the trade-off between the number of regulation loops, line regulation, and supply range. Increasing the number of regulation loops from N=1 (2T) to N=4 (5T) progressively reduces *LR*, while the minimum usable supply voltage V_{setup} rises by approximately 2.3 V per added loop, thus reducing the usable supply range $V_{DD,range} = V_{DD,max} - V_{setup}$. At N=3 (4T), *LR* reaches an extremely low level, whereas $V_{DD,range}$ remains wide (approximately 7.3~50 V), representing the best trade-off between *LR* suppression and supply flexibility.

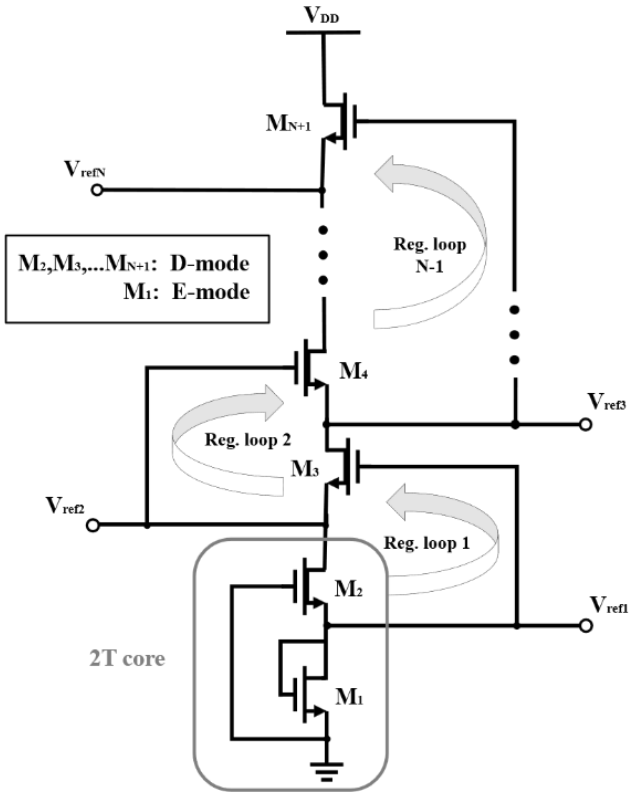


Fig. 3. Schematic structure of multi-loop regulating circuit.

Furthermore, closed-form analytical derivations provide three key circuit parameters (V_{ref1}, *LR*, and V_{setup}) that are presented to support the simulation findings and to provide design guidance for further engineering optimization.

A. Reference Voltage (V_{ref1})

The reference voltage, which comes from the 2T-core, can be defined as V_{ref1}. When M_2 is operating in the saturation region, ignoring the leakage current in M_2 and M_1, the source current output from M_2 will be the same as the drain current flowing into M_1. In reference to the compact mode for MIS-HEMTs [11], the drain current is concluded as

$$I_{D,Sat} = \frac{1}{2}\mu_{eff}C_{eff}\frac{W}{L}(V_{GS} - V_{th})^2 \quad (1)$$

where the μ_{eff} is the effective mobility, C_{eff} is the effective capacitance, and W/L is the ratio between the channel width and length. Considering $I_{D,M1,E} = I_{D,M2,D}$, and $K_{n,E}/K_{n,D} = \mu_{eff,E}C_{eff,E}/\mu_{eff,D}C_{eff,D}$, so it is possible to get a voltage relationship from those equations:

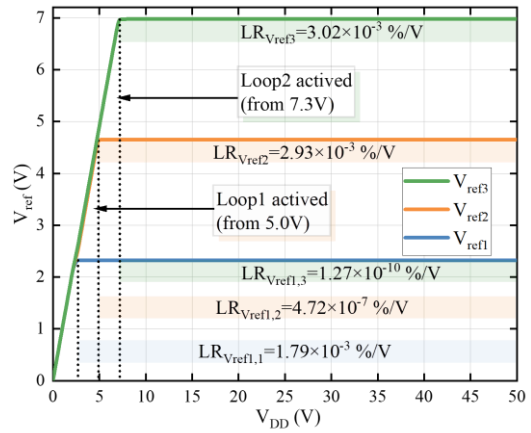
$$\frac{1}{2}K_{eff,E}\left(V_{gs,E} - V_{th,E}\right)^2 = \frac{1}{2}K_{eff,D}\left(V_{GS,D} - V_{th,D}\right)^2 \quad (2)$$

where $V_{GS,M1} = V_{ref1}$, thus, it can be rewritten as

$$V_{ref1} = \frac{\sqrt{\frac{K_{n,E}}{K_{n,D}}} \times V_{th,E} - V_{th,D}}{1 + \sqrt{\frac{K_{n,E}}{K_{n,D}}}} \quad (3)$$

which is only controlled by the ratio of conductance coefficients and their threshold voltages.

(a)



(b)

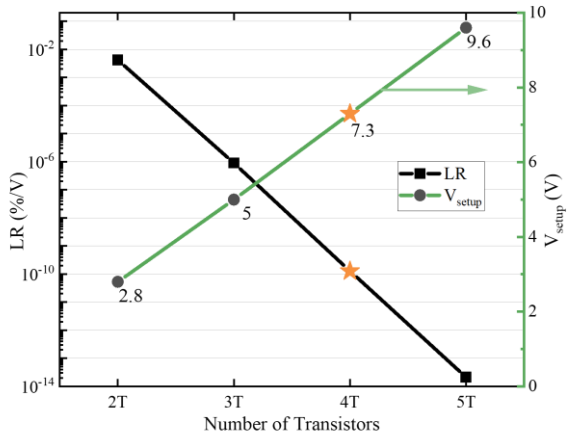


Fig. 4. (a) The simulation result diagram of 4T multi-loop VR. (b) *LR* of V_{ref1} and minimum operating voltage versus number of transistors.

B. Line Regulation (*LR*)

Based on a small signal module, in a 2T-core, the relationship between voltage changes can be written as

$$\Delta V_{ref1} = \Delta I_{D,M1} \times r_{d1} \tag{4}$$

Since the drain and source current changes from M_1 and M_3 are the same and the source current is equal to the ratio of ΔV_{DD} over r_{o2} (where the r_{o2} is equal to r_{ds}), return to the definition of linear regulation $LR = \Delta V_{out}/\Delta V_{in}$, where ΔV_{out} at here is ΔV_{ref1} and ΔV_{in} is ΔV_{DD}, the *LR* of 2T can be rewrite as

$$LR_{2T} = \frac{1}{2g_{m1}r_{ds}} \tag{5}$$

When its transistors increase to 3T even more, assuming the r_{ds} of each added transistor is the same and the number of the D-mode transistors is N, the *LR* of the first stage of voltage output at (N+1)T structure can be defined and extended as

$$LR_1 = \frac{\Delta V_{ref1}}{\Delta V_{DD}} = \frac{\prod_{i=1}^{N} \Delta V_{refi}}{\Delta V_{DD} \times \prod_{i=2}^{N} \Delta V_{refi}} \tag{6}$$

Focusing on the last term in this equation, $\Delta V_{refN}/\Delta V_{DD}$ can be isolated and rewritten as $g_m r_{ds}$, since these D-mode transistors are in series where their drain and source currents are the same. It is easy to discover that if the topmost D-mode transistor is removed, the coefficient $g_m r_{ds}$ still exists in the last term in this equation. By removing the transistor several times, it indicates that for each additional D-mode transistor, the value of *LR* will increase by $g_m r_{ds}$ times. For the first V_{ref} in (N+1) T structure, the *LR* of V_{ref1} can be rewritten as:

$$LR_1 = \frac{\Delta V_{ref1}}{\Delta V_{DD}} = \frac{1}{2g_{m1}r_{ds}(g_m r_{ds})^{N-1}} \tag{7}$$

TABLE 1. PERFORMANCE SUMMARY AND COMPARISON

	This work (simulation)		EDL 2022 [3]	ISSSCC 2020 [6]	TCAS 2019 [12]
Process	GaN MIS-HEMT		GaN MIS-HEMT	p-GaN	CMOS
$V_{DD,range}$ (V)	2.8~50	7.3~50	4.8~50	3.9~24	0.7~2.0
V_{ref} (V)	2.33		2.53	3.19	0.368
LS (%/V)	1.79 $\times 10^{-3}$	1.27 $\times 10^{-10}$	0.063	0.32	0.027
V_{setup} (V)	2.8	7.3	4.8	3.9	0.7

C. Start-up Voltage (V_{setup})

As mentioned in the working principle, the value relation between the last V_{ref} and the first V_{ref} is

$$V_{refN} = NV_{ref1} \tag{8}$$

The start-up voltage is the minimum supply voltage in this circuit, which is defined as the sum of the saturation voltage of the D-mode transistor and the value of the last V_{ref} in the circuit:

$$V_{setup} = V_{DS,sat} + V_{refN} \tag{9}$$

Therefore, the saturation voltage of the top D-mode transistor can be expressed as the difference between its gate–source drive and its threshold, which means $V_{DS,sat} = V_{GS,N+1} - V_{th,D} = -V_{ref1} - V_{th,D}$, so start up voltage can be rewrite as

$$V_{setup} \approx (N-1)V_{ref1} - V_{th,D} \tag{10}$$

where N is the number of D-mode transistors in this circuit.

In Table 1, several voltage reference implementations in both GaN and Si CMOS technologies are compared. The present work offers the following notable advantages: it supports a relatively wide supply range (approximately 7.3~50 V), making it suitable for relatively high voltage/wide-range applications, and provides a stable 2.33 V reference across this wide supply range, reducing the need for additional level shifting or buffering. This work exhibits relative the best stability against supply variations among the state-of-the-art.

IV. Conclusions

This work conducted circuit-level simulations in ADS using the AlGaN/GaN MIS-HEMT ASM model. The 4T multi-loop topology provides a stable 2.33 V reference across a 2.8~50 V supply range while substantially reducing line sensitivity, demonstrating a favorable trade-off between line regulation and supply flexibility. Closed-form expressions for V_{ref1}, *LR*, and V_{setup} are derived, offering practical design guidance for GaN-based reference circuits.

Acknowledgments

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